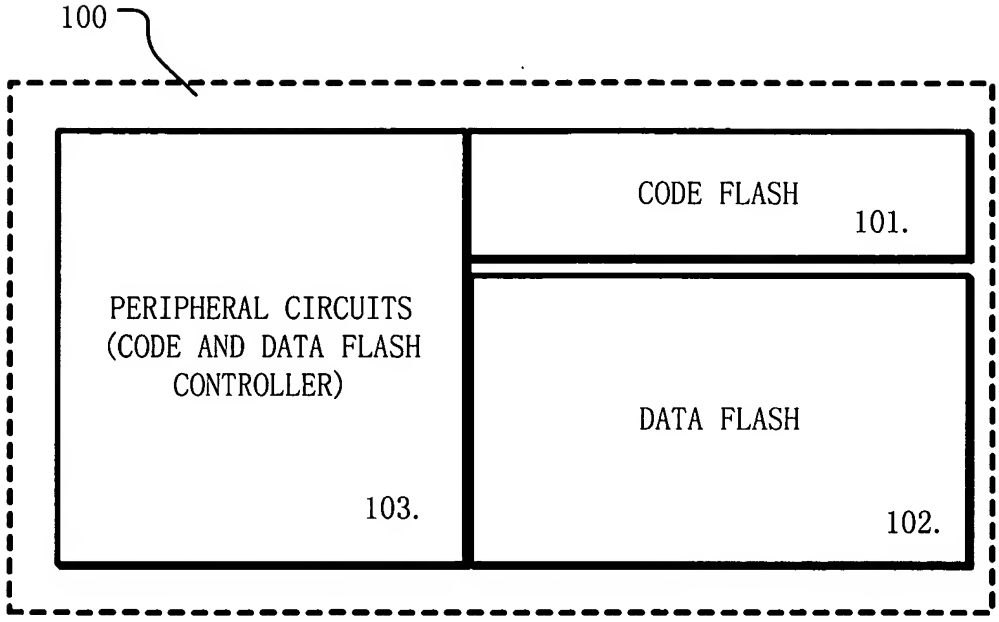

100
PERIPHERAL CIRCUITS
(CODE AND DATA FLASH
CONTROLLER)
103.
CODE FLASH
101.
DATA FLASH
102.

FIG. 1

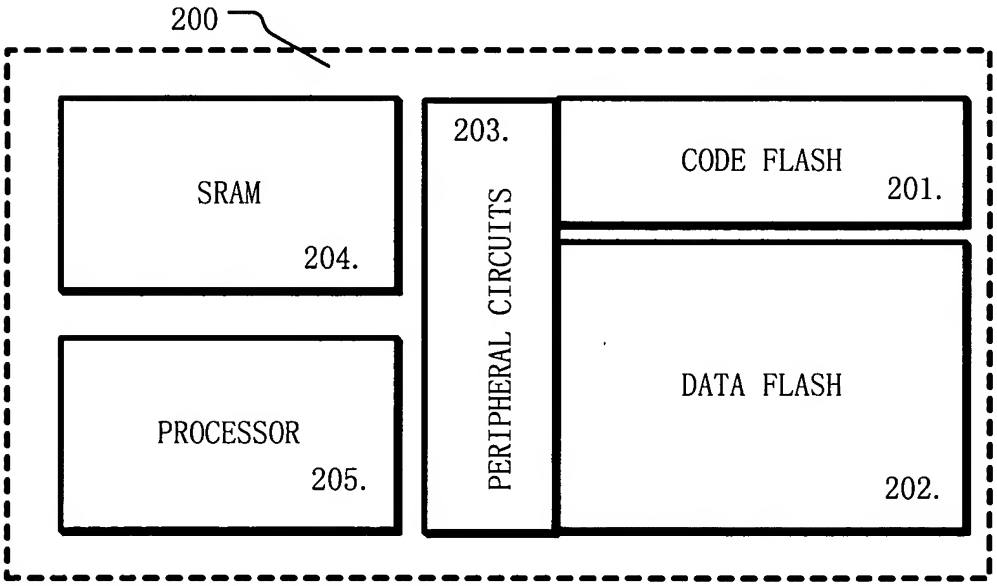

200
SRAM
204.
PROCESSOR
205.
203.
PERIPHERAL CIRCUITS
CODE FLASH
201.
DATA FLASH
202.

FIG. 2

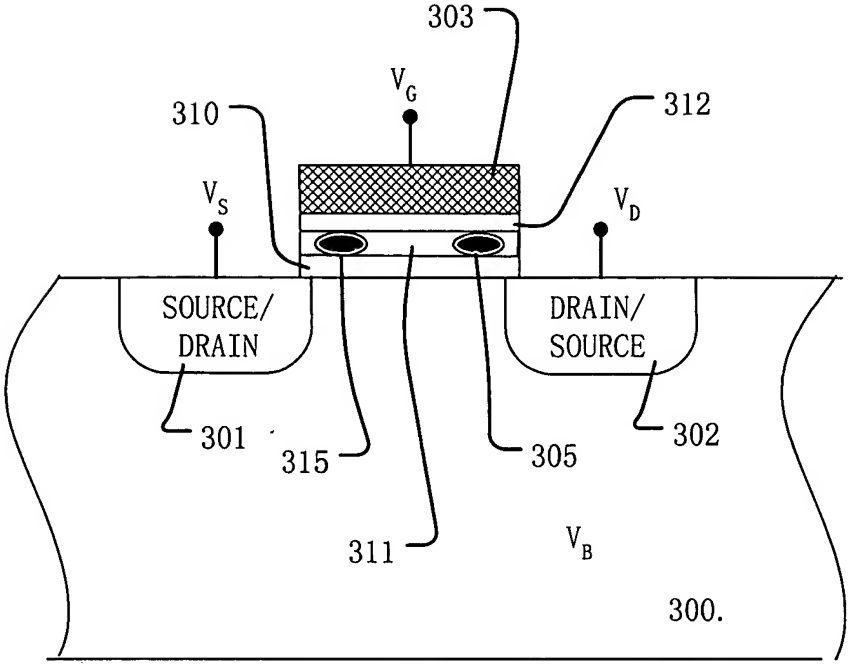

303
V_G
310
312
V_S
V_D
SOURCE/
DRAIN
DRAIN/
SOURCE
301
315
305
302
311
V_B
300.

FIG. 3

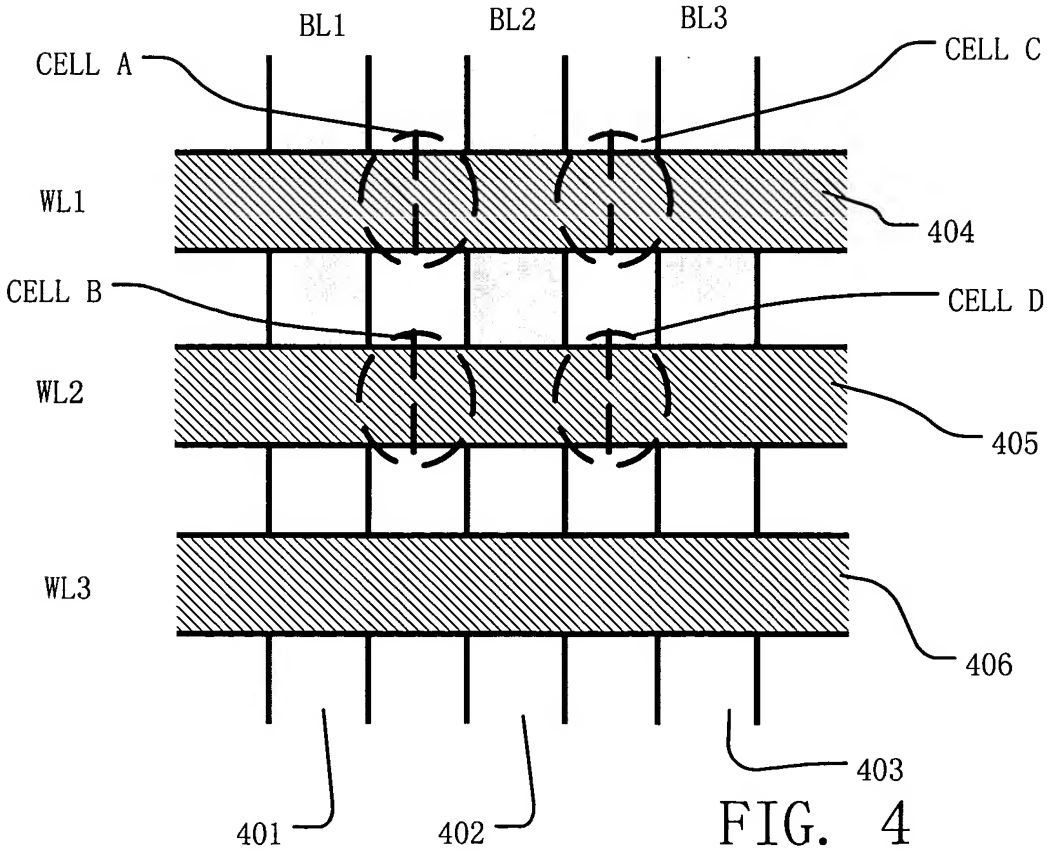
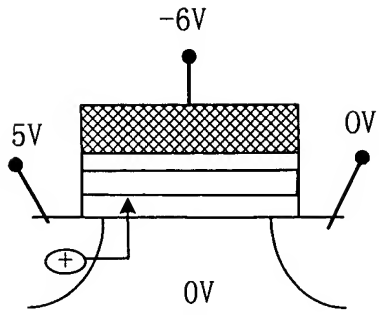

BL1
BL2
BL3
CELL A
CELL C
WL1
404
CELL B
CELL D
WL2
405
WL3
406
401
402
403

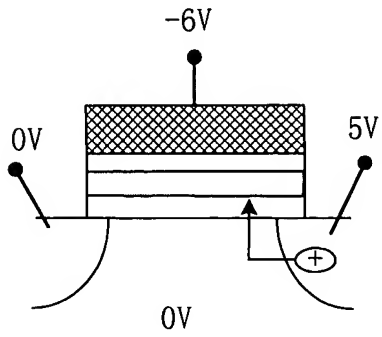
FIG. 4

FIG. 5A



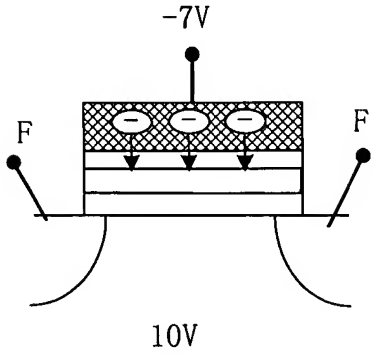
DATA PROGRAM
(LEFT BIT)

FIG. 5B



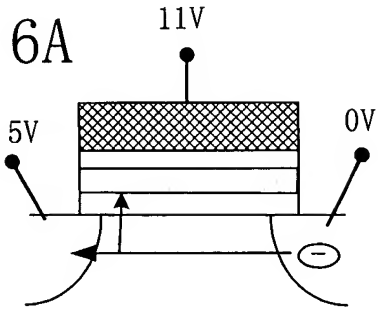
DATA PROGRAM
(RIGHT BIT)

FIG. 5C



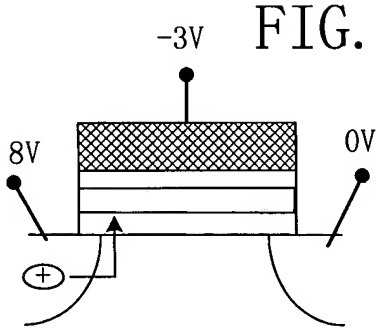
DATA ERASE
(BOTH BITS)

FIG. 6A



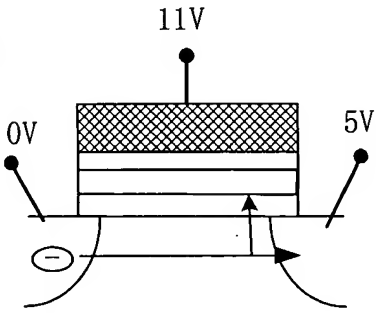
CODE PROGRAM
(LEFT BIT)

FIG. 6C



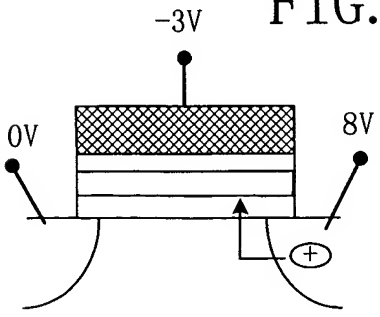
CODE ERASE
(LEFT BIT)

FIG. 6B



CODE PROGRAM
(RIGHT BIT)

FIG. 6D



CODE ERASE
(RIGHT BIT)

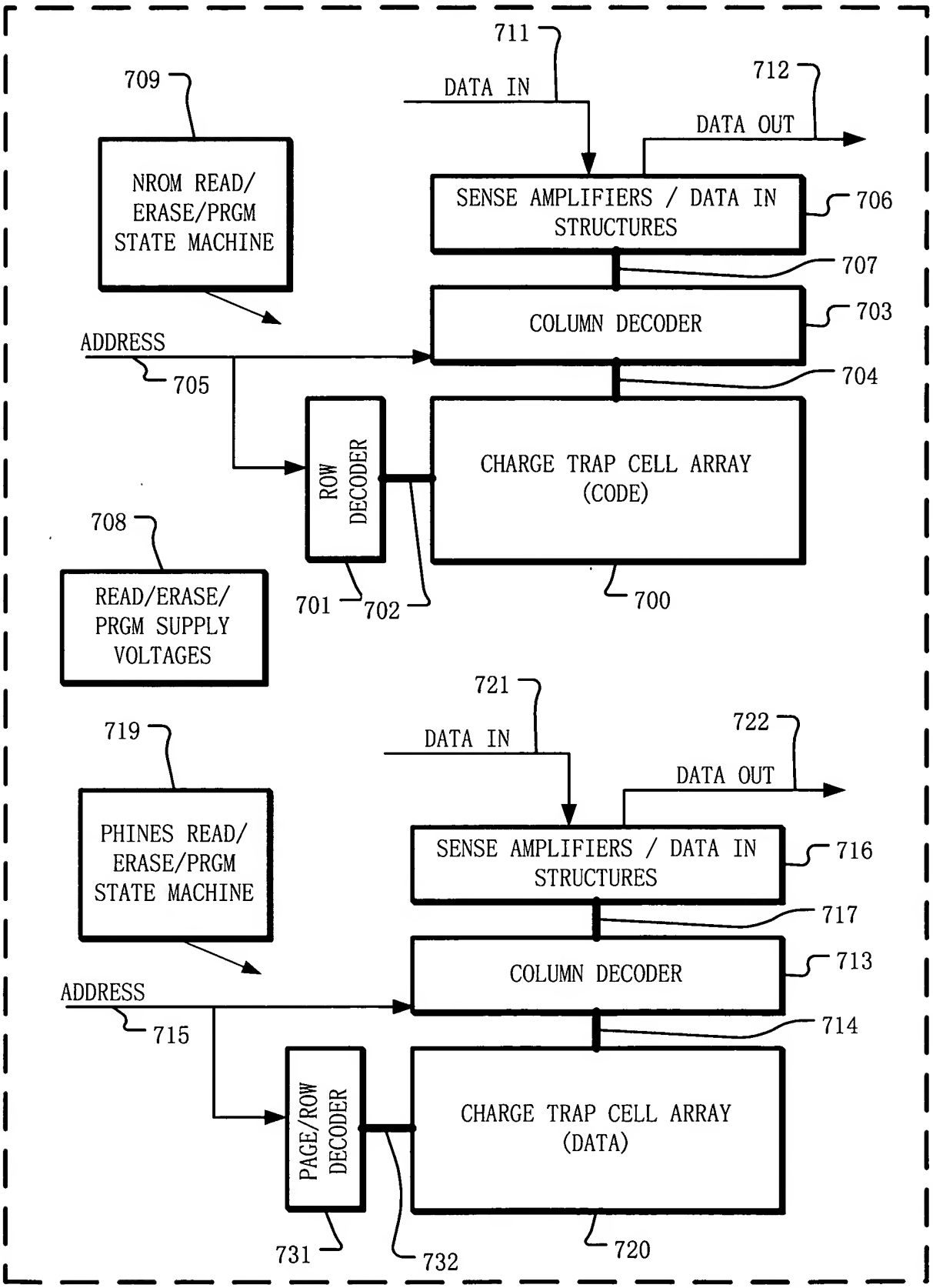

711
DATA IN
712
DATA OUT
709
NROM READ/ ERASE/PRGM STATE MACHINE
SENSE AMPLIFIERS / DATA IN STRUCTURES
706
707
COLUMN DECODER
703
ADDRESS
705
704
ROW DECODER
CHARGE TRAP CELL ARRAY (CODE)
708
READ/ERASE/ PRGM SUPPLY VOLTAGES
701
702
700
721
DATA IN
722
DATA OUT
719
PHINES READ/ ERASE/PRGM STATE MACHINE
SENSE AMPLIFIERS / DATA IN STRUCTURES
716
717
COLUMN DECODER
713
ADDRESS
715
714
PAGE/ROW DECODER
CHARGE TRAP CELL ARRAY (DATA)
731
732
720

FIG. 7